

MOS FIELD EFFECT TRANSISTOR NP82N06PLG

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The NP82N06PLG is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

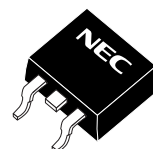
PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP82N06PLG-E1-AY ^{Note}	Pure Sn (Tin)	Tape 800 p/reel	TO-263 (MP-25ZP)
NP82N06PLG-E2-AY ^{Note}			

Note Pb-free (This product does not contain Pb in the external electrode.)

FEATURES

- Super low on-state resistance
 $R_{DS(on)1} = 6.7 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 41 \text{ A)}$
 $R_{DS(on)2} = 8.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 5 \text{ V, } I_D = 41 \text{ A)}$
- Low input capacitance
 $C_{iss} = 5700 \text{ pF TYP.}$
- Built-in gate protection diode

(TO-263)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	60	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±82	A
Drain Current (pulse) ^{Note1}	I _{D(pulse)}	±270	A
Total Power Dissipation (T _C = 25°C)	P _{T1}	143	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.8	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-55 to +175	°C
Repetitive Avalanche Current ^{Note2}	I _{AR}	37	A
Repetitive Avalanche Energy ^{Note2}	E _{AR}	137	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. T_{ch} ≤ 150°C, V_{DD} = 30 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

THERMAL RESISTANCE

Channel to Case Thermal Resistance	R _{th(ch-C)}	1.05	°C/W
Channel to Ambient Thermal Resistance	R _{th(ch-A)}	83.3	°C/W

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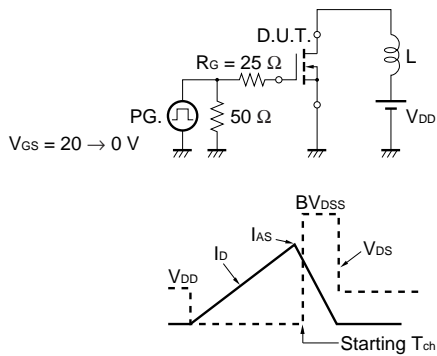
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

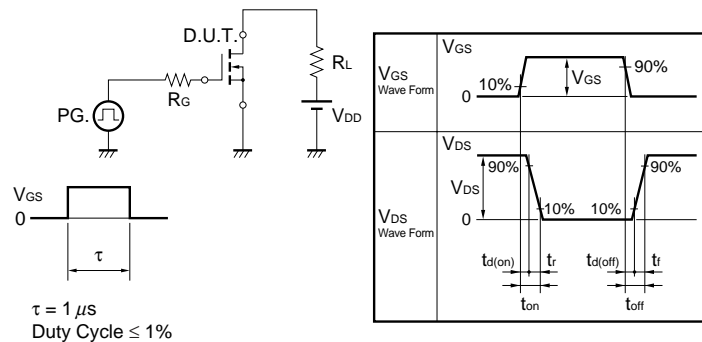
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate to Source Threshold Voltage ^{Note}	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 41 A	19	40		S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 10 V, I _D = 41 A		5.1	6.7	mΩ
	R _{DS(on)2}	V _{GS} = 5 V, I _D = 41 A		6.4	8.5	mΩ
Input Capacitance	C _{iss}	V _{DS} = 25 V,		5700	8550	pF
Output Capacitance	C _{oss}	V _{GS} = 0 V,		420	630	pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		275	500	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 30 V, I _D = 41 A,		28	70	ns
Rise Time	t _r	V _{GS} = 10 V,		22	60	ns
Turn-off Delay Time	t _{d(off)}	R _G = 0 Ω		79	160	ns
Fall Time	t _f			9	30	ns
Total Gate Charge	Q _G	V _{DD} = 48 V,		106	160	nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V,		29		nC
Gate to Drain Charge	Q _{GD}	I _D = 82 A		35		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 82 A, V _{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 82 A, V _{GS} = 0 V,		43		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		65		nC

Note Pulsed

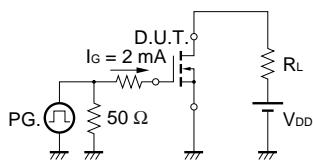
TEST CIRCUIT 1 AVALANCHE CAPABILITY



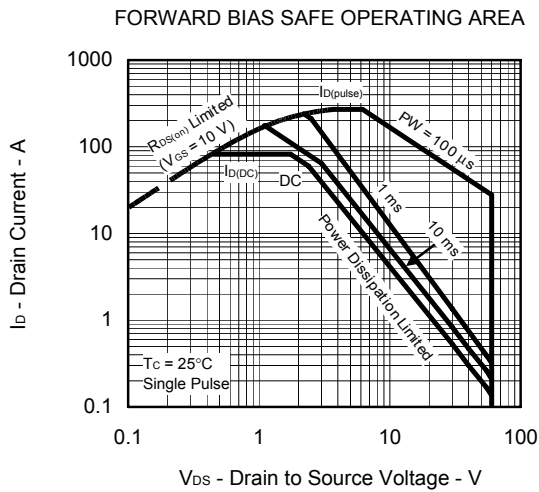
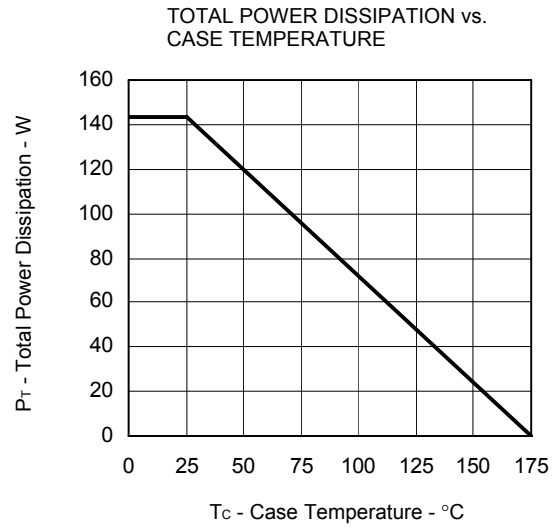
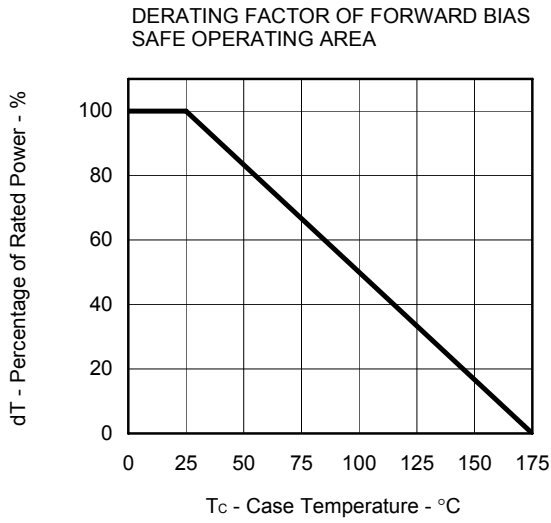
TEST CIRCUIT 2 SWITCHING TIME



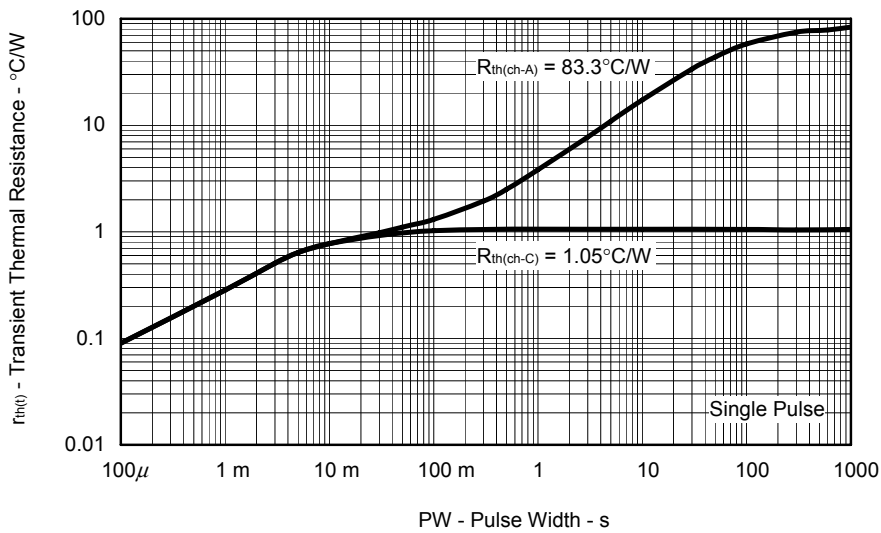
TEST CIRCUIT 3 GATE CHARGE



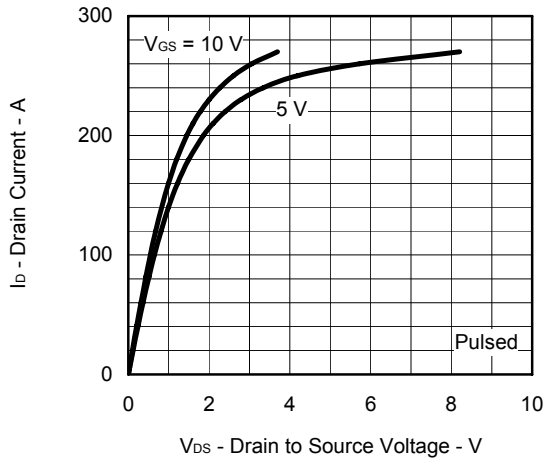
TYPICAL CHARACTERISTICS (T_A = 25°C)



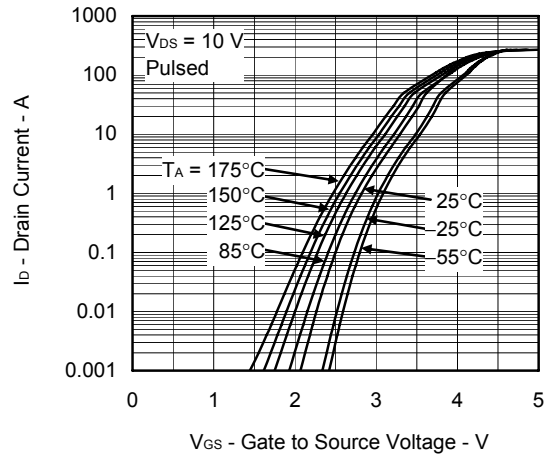
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



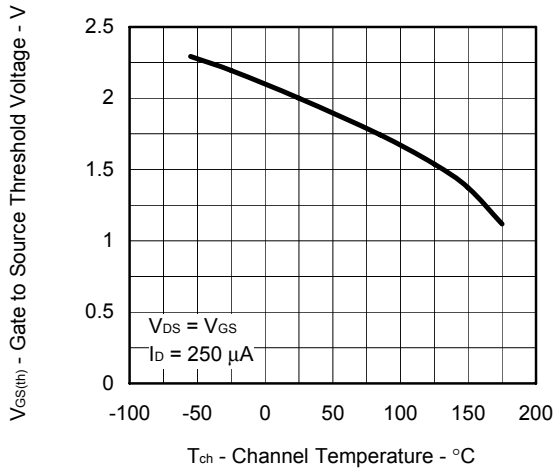
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



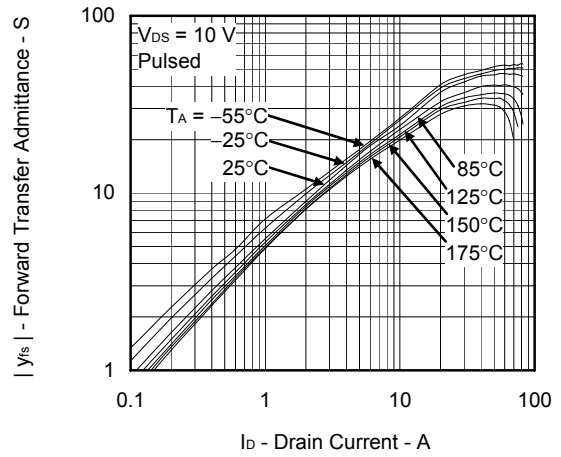
FORWARD TRANSFER CHARACTERISTICS



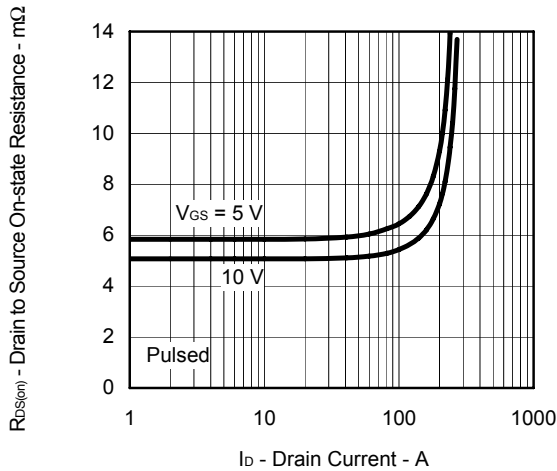
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



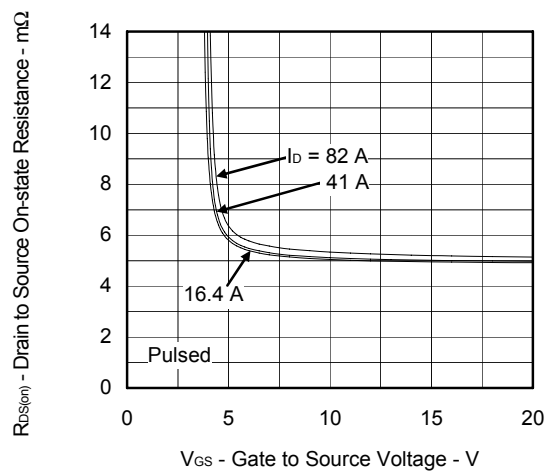
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



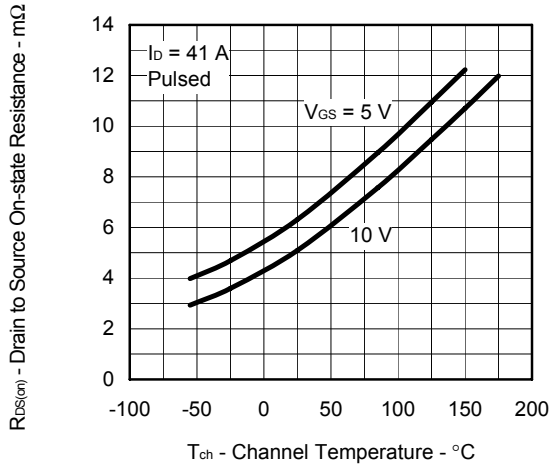
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



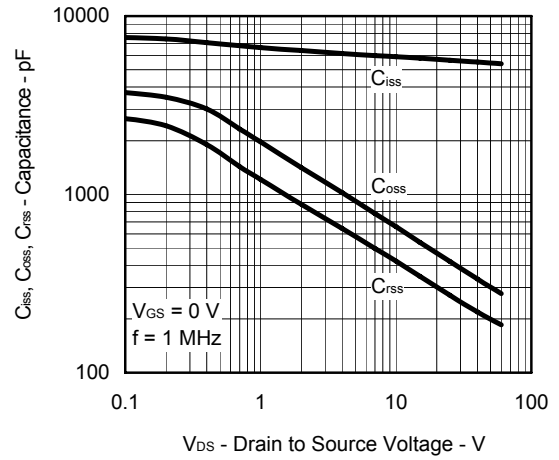
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



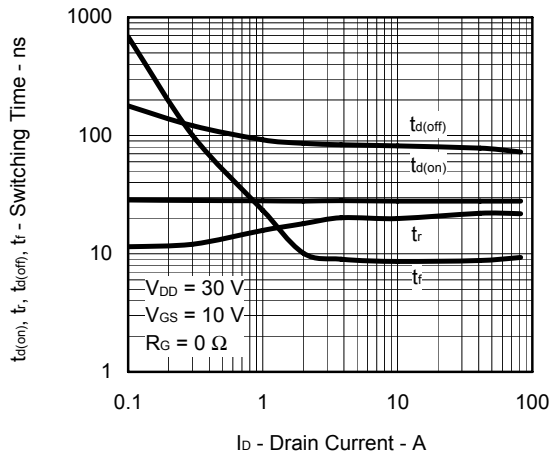
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



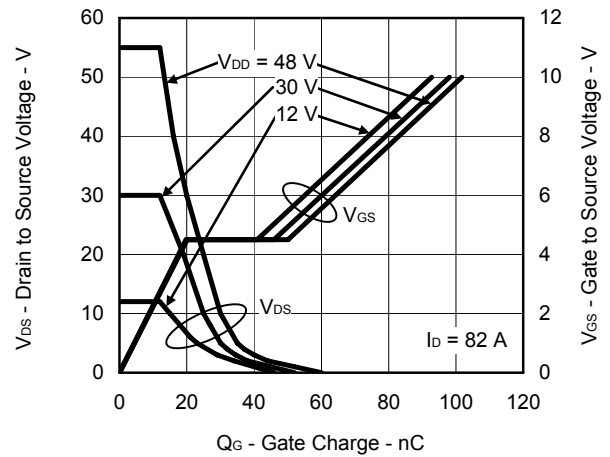
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



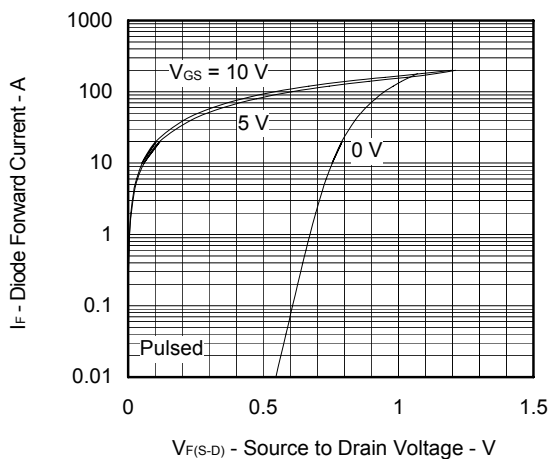
SWITCHING CHARACTERISTICS



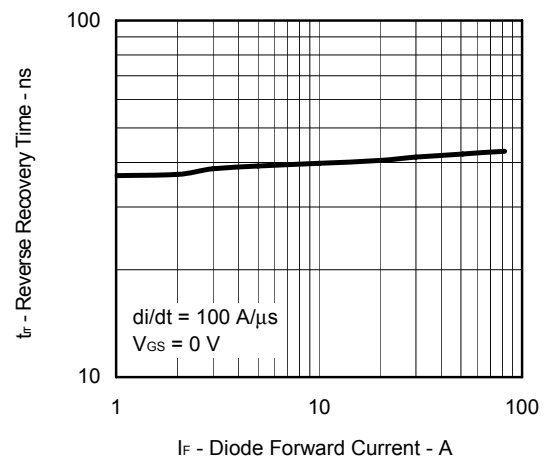
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

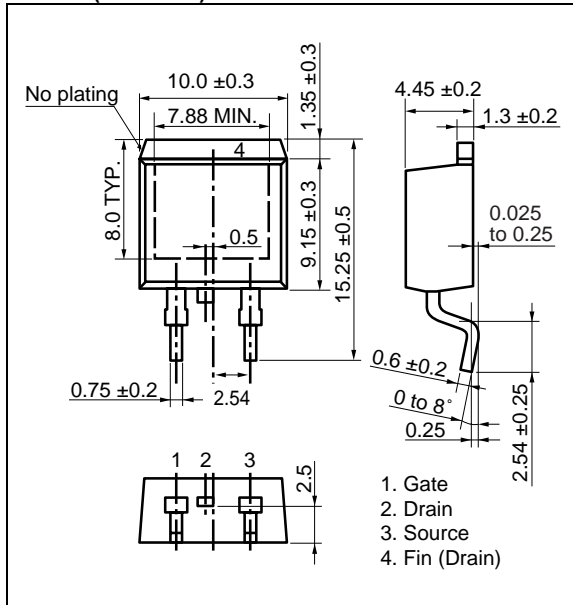


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

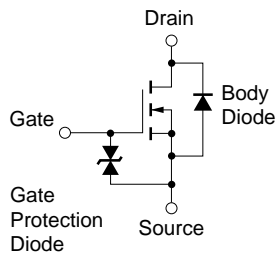


PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZP)



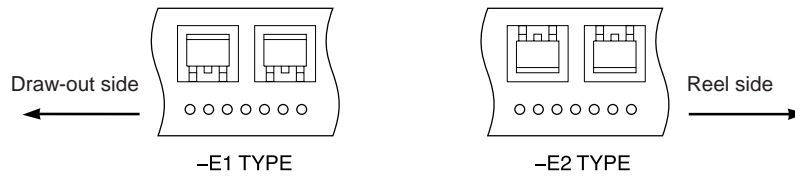
EQUIVALENT CIRCUIT



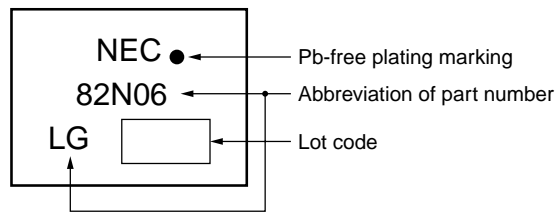
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The NP82N06PLG should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Partial heating	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution Do not use different soldering methods together (except for partial heating).

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